ABSTRACT

A self-aligned transistor including a first silicon portion on an isolation layer, the silicon portion having formed therein a source region and a drain region separated by a channel region. The channel region has a first side and a second side and a top portion, and a gate oxide surrounds the channel on said first side, second side and top portion. A first, a second and a third silicon gate regions are positioned in a second silicon portion surrounding the first silicon portion about the first side, second side and top portion and the channel region.

Also disclosed is a method for manufacturing a transistor device. The method for manufacturing includes the steps of: providing a substrate having a buried oxide region; depositing a first nitride mask layer having a pattern overlying a silicon region; forming a trench in said substrate with a depth to said buried oxide; depositing a conformal oxide in said trench; forming vias in said conformal oxide adjacent to said silicon region and removing a portion of said first nitride mask to expose a portion of said silicon region; depositing polysilicon in said vias and on said portion of said silicon region; and implanting an impurity into exposed portions of polysilicon in said trench and of said silicon-on-insulator substrate underlying said second nitride layer.